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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/047,121 | 01/15/2002 | Brian Keith Owens | 2001-0273.00 | 1297 |

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| EXAMINER | |
|---|---|
| KANG, ROBERT N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2622 | |

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/047,121 | OWENS ET AL. | |
| | Examiner | Art Unit | |
| | Robert N. Kang | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11 and 13* is/are rejected.

7)☒ Claim(s) *6,12 and 14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date [redacted] 12-21-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's arguments, see page 11, paragraph 3, filed 1/15/06, with respect to claims 5, 11, and 17 have been fully considered and are persuasive in light of the attached Amtel reference. The 35 U.S.C. § 112 rejections of claims 5, 11, and 17 has been withdrawn.

2. Applicant's arguments, see page 12, paragraph 2, filed 1/15/06, with respect to claim 13 have been fully considered and are persuasive. The misunderstanding occurred when the Examiner mistakenly took the invention to have both the non-ROM and the ROM memory manufactured at the same time; now it is clear that the ROM is burned and manufactured with the final code after the debugging in the temporary memory. The 35 U.S.C. § 112 rejection of claim 13 has been withdrawn.

3. Independent claims 1, 7, and 13 have been amended such that they now require " a non-ROM to ROM interface operatively connected to the ROM memory cells without any interposed RAM." This is new matter which was not supported in the specification and therefore claims are now rejected under 35 U.S.C. §112.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 7, and 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicant never disclosed in the specification that the invention excluded "any interposed RAM between the non-ROM to ROM interface." Differences between the two inventions are minimal at best, and therefore, the removal of the interposed RAM does not in any way entitle patentability.

***Claim Rejections - 35 USC § 102***

1. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Ali (US-PAT 6,016,472).

With regards to claim 1, Ali discloses in figure 3 a DSP 310, with its own integral ROM 312, communicably attached through serial interface 122 to a flash memory unit 120 having internal non-volatile storage 324. Broadly defined, a "memory module" is a self-contained device capable of storing digital data. Therefore, the entire invention as disclosed by Ali qualifies as a type of memory module. The program ROM 312 meets the criteria of limitation (a), since the recited memory module comprises "a read only memory (ROM memory) cells." Furthermore, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120, which qualifies as non-ROM. Therefore serial interface 122 is a "ROM to non-ROM interface," as required by limitation (b).

Regarding claim 2, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120, which qualifies

as an EPROM. Therefore serial interface 122 is a "ROM to EPROM interface." This is inconsistent with the generally accepted definition of an EPROM, which requires that the erase operation occur through the use of ultraviolet light. However, because the applicant's disclosed claim 3 identifies that Flash memory is an EPROM, the examiner is consistent with the applicant's strict interpretation of an EPROM as any memory which is erasable, programmable, and read-only.

Regarding claim 3, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120. Therefore serial interface 122 is a "ROM to Flash interface."

Regarding claim 4, because the program ROM 312 controls the DSP 310's operation and is encapsulated within the DSP block 110, the ROM 312 is operatively connected to the Flash memory unit 120 through serial interface 122. Therefore the "Flash to ROM interface is a serial interface."

In regards to claim 5, Ali details the various connections of serial interface 122 in figure 2. In column 5, lines 31-32, Ali states "a chip select (CS) input is driven to a low logic state to indicated the beginning of a command to the flash memory." This input qualifies as "a Flash chip select transmission line," as claimed in line 3. Ali discloses in lines 37-51, "a serial clock (SCK) input on the flash memory unit 120 is driven by a second bit input/output BIO1 on the DSP... A serial input (SI) line on the flash memory unit 120 is driven by a third bit input/output BIO2 on the DSP... A serial output (SO) line on the flash memory unit 120 drives a fourth bit input/output BIO3." These transmission lines are congruous to the "clock transmission line, flash serial input transmission line,"

and "flash serial output transmission line," as claimed in lines 2-3. Ali also discloses in column 5, lines 55-61, "a reset (RESET input on the flash memory unit 120 is coupled to the sixth bit input/out BIO6 on the DSP," which is identical to the function and operation of the applicant's disclosed "flash reset transmission line." Ali also describes "a ready/busy (RDY/BUSY) output from the flash memory unit 120 to a seventh bit input/output BIO6." This qualifies as "a status command." Finally, Ali depicts in figure 3 flash buffers 320 and 322, which serve to store input/output data. In column 10, lines 44-51, Ali states "data is passed from the DSP to the flash memory unit by setting the SI logic level appropriately before the SCK line is driven from low to high... data is passed from the flash memory unit 120 to the DSP 110 by setting the SO logic level appropriately before the SCK line is driven from low to high." These commands qualify as "read" and "write" commands for the Flash input transmission line.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima (US-PAT 6,250,827) in view of Ali (US-PAT 6,016,472).

Regarding claim 7, Nojima discloses in paragraph (249), "In FIG. 45, reference numeral 500 designates an ASIC in which the MPU part and printer control part are integrated. Numeral 504 represents a flash ROM which stores programs for controlling

the whole of the recording device, numeral 505 a mask ROM storing character fonts etc., and numeral 506 a DRAM used as a work area of the ASIC 500 and as a buffer of signal. Numeral 509 denotes an EEPROM, this EEPROM 509 being a rewritable ROM which can retain the contents without supply of power." Therefore Nojima's invention qualifies as "a printer-controller ASIC having non-ROM memory control."

Nojima does not disclose a "memory module including ROM memory cells and a non-ROM to ROM interface operatively connected to the ROM memory cells, and a transmission cable operatively connected to the non-ROM memory control of the printer controller ASIC and the non-ROM to ROM interface of the memory module."

Ali discloses in figure 3 a DSP 310, with its own integral ROM 312, communicably attached through serial interface 122 to a flash memory unit 120 having internal non-volatile storage 324. Broadly defined, a "memory module" is a self-contained device capable of storing digital data. Therefore, the entire invention as disclosed by Ali qualifies as a type of memory module. The program ROM 312 meets the criteria of limitation (a), since the recited memory module comprises "a read only memory (ROM memory) cells." Furthermore, Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120, which qualifies as non-ROM. Therefore serial interface 122 is a "ROM to non-ROM interface," as required by limitation (b).

Nojima and Ali are combinable because they both deal with ROM memory management in low cost devices such as printer ASICs and voice answering machines.

It would have been obvious at the time of invention to one of normal skill in the art to implement in Nojima's printing system Ali's memory module by replacing the DSP with the printer ASIC in the memory module block diagram.

The motivation of this modification would be to allow easy debugging and changes to the internal program memory of the print ASIC through the Flash Memory.

Therefore it would have been obvious to combine Nojima and Ali to achieve the invention of claim 7. For the purposes of convenience, for further rejections the above combination of the Nojima print ASIC containing the Ali memory module shall be referred to herein as the "Nojima/Ali combination."

In regards to claim 8, the Nojima/Ali combination contains serial interface 122, which connects the ROM 312 (via the printer ASIC), to the flash memory unit 120, which qualifies as an EPROM. Therefore serial interface 122 is a "ROM to EPROM interface." This is inconsistent with the generally accepted definition of an EPROM, which requires that the erase operation occur through the use of ultraviolet light. However, because the applicant's disclosed claim 3 identifies that Flash memory is an EPROM, the examiner is consistent with the applicant's strict interpretation of an EPROM as any memory which is erasable, programmable, and read-only.

Ali's disclosed invention contains serial interface 122, which connects the ROM 312 (via the DSP 310), to the flash memory unit 120. Therefore serial interface 122 is a "ROM to Flash interface."

Regarding claim 9, because in the Nojima/Ali combination, the program ROM 312 controls the ASIC's operation and is encapsulated within the ASIC block, the ROM

312 is operatively connected to the Flash memory unit 120 through serial interface 122. Therefore the "Flash to ROM interface is a serial interface."

In regards to claim 10, Ali details the various connections of serial interface 122 in figure 2, utilized between the ROM and Flash Memory of the Nojima/Ali combination. In column 5, lines 31-32, Ali states "a chip select (CS) input is driven to a low logic state to indicated the beginning of a command to the flash memory." This input qualifies as "a Flash chip select transmission line," as claimed in line 3.. Ali discloses in lines 37-51, "a serial clock (SCK) input on the flash memory unit 120 is driven by a second bit input/output BIO1... A serial input (SI) line on the flash memory unit 120 is driven by a third bit input/output BIO2... A serial output (SO) line on the flash memory unit 120 drives a fourth bit input/output BIO3." These transmission lines are congruous to the "clock transmission line, flash serial input transmission line," and "flash serial output transmission line," as claimed in lines 2-3. Ali also discloses in column 5, lines 55-61, "a reset (RESET input on the flash memory unit 120 is coupled to the sixth bit input/out BIO6 on the DSP," which is identical to the function and operation of the applicant's disclosed "flash reset transmission line." Ali also describes "a ready/busy (RDY/BUSY) output from the flash memory unit 120 to a seventh bit input/output BIO6." This qualifies as "a status command." Finally, Ali depicts in figure 3 flash buffers 320 and 322, which serve to store input/output data. In column 10, lines 44-51, Ali states "data is passed from the DSP to the flash memory unit by setting the SI logic level appropriately before the SCK line is driven from low to high... data is passed from the flash memory unit 120 to the DSP 110 by setting the SO logic level appropriately before the SCK line is driven

from low to high." These commands qualify as "read" and "write" commands for the Flash input transmission line, and are applicable in the Nojima/Ali combination wherein the printer ASIC replaces the DSP.

4. Claims 6, 12, 14-18 are objected to as being dependent upon a rejected base claim.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert N. Kang whose telephone number is (571) 272-0593. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Coles can be reached on (571)272-7402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RNK

TWYLER LAMB
PRIMARY EXAMINER